MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Quarterly Report #13

(Contract NIH-NINDS-NO1-NS-9-2304)

April - June 2002

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

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Ann Arbor, Michigan
48109-2122

July 2002

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400µm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. This probe design has now been completed, with 3D arrays of the STIM-3B probes formed in arrays as large as 1024 sites (256 shanks and 64 parallel data channels, accessible over just eleven external leads). The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters. They are accessible over seven external leads.

During the past quarter, work has gone forward in two principal areas. We have explored approaches to reducing the circuit on our high-end stimulating probes, and we have continued in our efforts to develop a wireless interface to these probes. There has been substantial progress in both areas. A chip containing the circuitry for a two-channel 16-site active probe has been designed in a 1.5µm n-well 2M/2P CMOS process and submitted to MOSIS for fabrication. This chip will be useful with passive stimulating probes, both in acute implementations (mounted on the supporting stalk) and in chronic use (on the platform). It will also serve to confirm the operation of several important circuit blocks. The chip contains five operating modes: site activation, impedance tests, normal stimulation, recording, or anodic bias set. Each command consists of 16 serial bits. We have also designed a four-channel 32-site active probe for fabrication this fall. It incorporates extensive self-test capability, current-output digital-to-analog converters that are much smaller in layout area and that incorporate a shared bias string whose current levels are independent of bias.

In the wireless area, we have continued to test the most recent circuit chips at very high data rates. The circuitry can generate an on-chip clock at 4MHz with power dissipation of about 0.5mW, following the carrier from 2MHz to 6MHz. The data recovery circuit performs well at 100kbit/sec data rates, and likely much higher. The dc-level shifter circuitry correctly produces voltages at 5V and 10V, consistent with using a 10V power supply swing to produce ±5V biphasic stimulus signals. The power-on-reset function is likewise fully functional. The digital control block permits internal clocks from 8.3kHz to 125kHz to be derived from the 4MHz input carrier. It also performs parity checking on the serial data bit stream from the data recovery block and formats the data together with a strobe for use by the probe circuitry. In order to test this circuitry, a PC-based command generator has been implemented. This system will also be important in testing the full wireless probe system, which we hope to do during the fall quarter.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A

new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have focused work on reducing the circuit size for the STIM-2 and STIM-3 probes as well as the realization of the first wireless interface for them. The results of these efforts are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

As noted in earlier reports, the full 64-site 8-channel active probe with on-chip current generation experienced high background currents and will be re-fabricated after layout changes. In addition, the circuit area on this probe was higher than desired for a chronic assembly, especially for use in small animals. We have therefore focused our attention on reducing the circuit area and on fabricating smaller versions of this probe. Folding the circuitry down on the platform will also be explored to reduce brain-skull clearance and hermetic sealing of a glass cap over the 3D microassembly will be investigated. During the past quarter, a MOSIS chip has been designed and submitted for fabrication. This chip contains the circuitry of a 2-channel, 16-site probe and is a modified version of the old circuit design. The purposes for designing this chip are: 1) to use the AMI 1.5µm process provided by MOSIS to explore how the backend circuit areas of these probes can be scaled down; 2) to obtain a chip that can be bonded and used with passive probes having different numbers of shanks and different site distributions; and 3) to obtain important information about the performance of various circuit blocks.

For this chip, the timing protocols and mode designations have been simplified from the last design. Thus, only one word of data is used in a command operation as shown in Fig.1. Accordingly, there are just four basic function modes the circuitry can perform; they are listed in Fig. 2. During power-on reset, the default mode is set to 00. As in STIM-2B, site-activation is also enabled at this time. Thus, the 00 mode is assigned for site activation, under which mode there is a direct path established from the sites to the output. For site-activation, the 16 sites are connected together to the output (previous experiments with STIM-2B have shown that this is an appropriate way to activate 16 sites simultaneously. During normal probe operation, any specific site can be connected to the output for site impedance tests or for use with an external, current source as in STIM-2B. In this case, the probe simply acts to steer the external currents to the selected sites. In the other three modes, the probe can be used for normal stimulation using the two active on-chip current sources, the two selected sites can be used for

recording, or anodic bias can be selected and specified. These are the important modes from the 64-site probe.

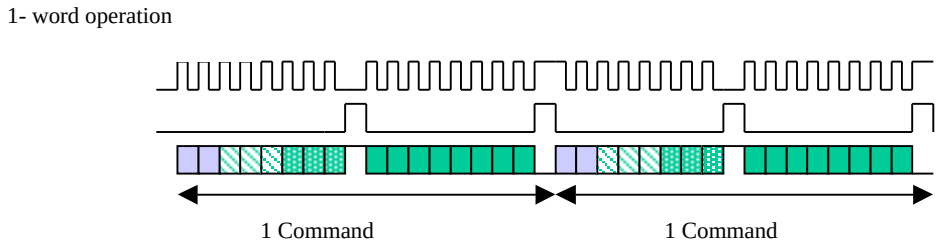


Fig. 1: Timing diagram for the circuitry

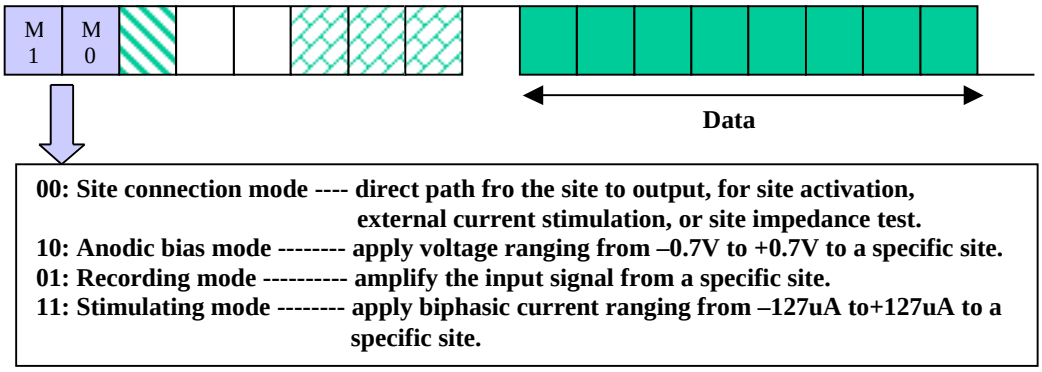


Fig. 2: Data designations for the circuitry of the 16-site probe chip

For the stimulating mode, the same high-swing cascoded current source is used in this design that was used on the latest version of STIM-2. A SPICE BSIM3 model provided by MOSIS was used for simulation, and it is expected to provide results that better match the experimental results. The previous amplifier design turned out to be unusable, since the two diode-connected NMOS transistors in that design have their substrates connected to ground. This works for isolated P-wells in a P-well process, but not for the AMI N-well process using a P-substrate and P-epi layer. The new amplifier design is shown in Fig 3. As in the old design, it uses a capacitor ratio to obtain the required AC gain. The only difference is the feedback MOSFET, which combined with the capacitors sets the lower cutoff frequency. The gate bias is set to 0.15V to obtain a lower frequency of ~1Hz. This bias is also connected to an external bonding pad so that the bias (and cutoff frequency) is externally tunable. The SPICE simulation is shown in Fig. 4. The mid-band gain is 40dB. Some specifications of the amplifier are listed in Table 1.

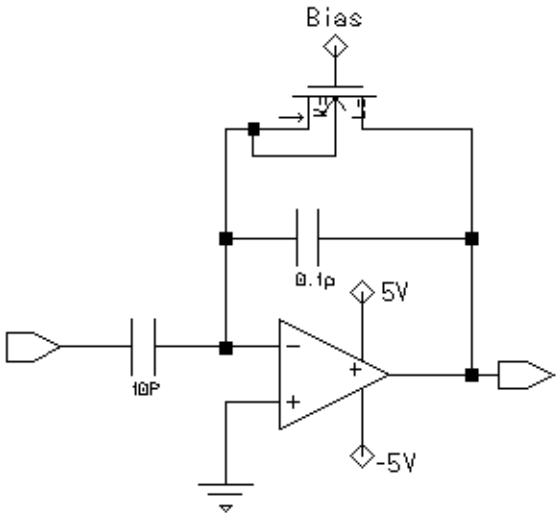


Fig. 3: Schematic of the amplifier used on the 16-site probe circuit.

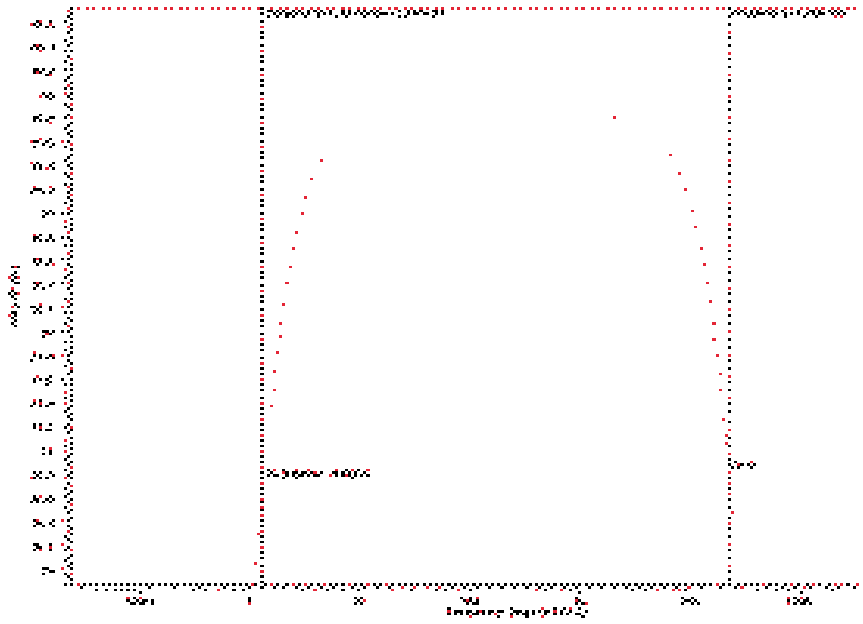


Fig. 4: SPICE simulation results for the amplifier on the 16-site probe circuitry.

Gain	40dB
Bandwidth	1Hz~20kHz
Power consumption	390uW
Input referenced noise	3.07uV

Table 1: Specifications for the amplifier on the 16-site probe chip.

The anodic voltage DAC is shown in Fig. 5. The left block represents a 3-bit current DAC using the same design as the stimulating current source. A 100kΩ resistor is used to transfer the output current into a voltage, and a source-follower-connected opamp is used to obtain a low output impedance. As the coded current DAC delivers current ranging from –7μA to +7μA, the output voltage swings from -0.7V to +0.7V.

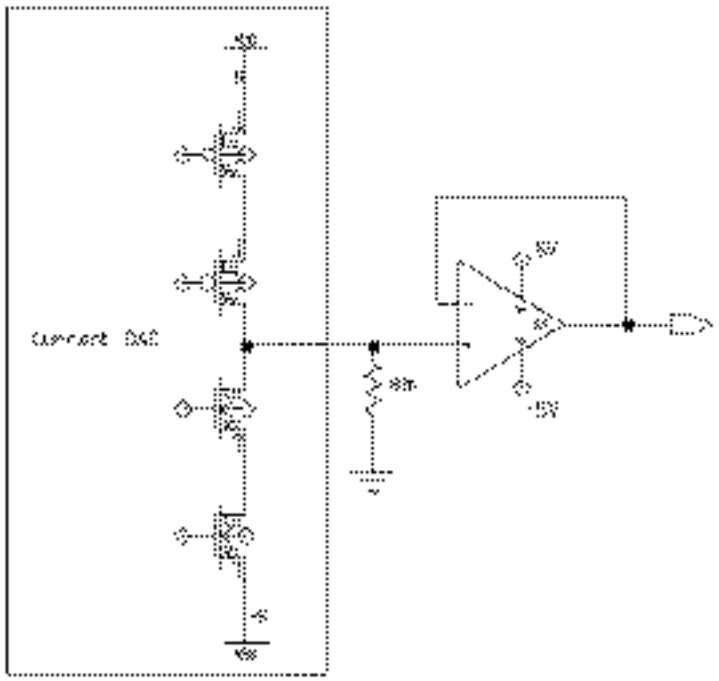


Fig. 5: Schematic of the anodic bias circuitry on the 2-channel 16-site MOSIS chip

The circuitry has been laid out in a 2mm by 2mm chip as shown in Fig. 6. The AMI process has 2 layers of metal and 2 layers of poly. The probe circuit area consumes about 1.9mm by 1.5mm and the rest is test circuitry. Thus, even with 1.5μm feature sizes and double metal layer, if 8-channel probes are desired, the circuit area is still a concern and a key factor in limiting probe scaling.

This chip is currently being fabricated and chips are expected to be ready for testing in early August. Since the P-substrate must to be connected to –5V when bonded with passive probe, the chip substrate must be isolated from the probe substrate. This is not expected to be a problem. For acute use, the chip can be mounted on the PCB stalk just behind the passive probe. For chronic use, it could be mounted on the rear area of the probe itself, potting it as is normally done there.

A new CMOS run is going to be initiated in the UM lab in September; therefore, a new probe design for this run is underway. A four-channel, 32-site probe is being designed for this run that incorporates a number of new features. Normally, a single

interconnect line is used on a given shank to check for shank breakage. This line is returned from the tip site, with continuity indicating an intact shank. Since on this eight-shank probe there will be only four sites on each shank, there is enough space to route every poly interconnect line leading to a specific site back to the circuitry, forming a loop as shown in Fig. 7. This can greatly simplify the site connection process and provide site information even after implantation. That is, it allows the connection between the poly and the site metal to be measured at any time and provides redundancy in accessing the sites. Another modification introduced on this probe concerns the current DAC. A kT/q reference bias string is used instead of the former bias string. This provides a much more stable bias current that is highly independent of power supply variations. Also, different sized transistors will be used to scale the output currents of the DAC instead of using parallel transistors of the unit size. This will sacrifice some linearity and accuracy, but the DAC layout area can be dramatically reduced. Due to area limitations (3µm feature sizes and single metal is used here), only one recording amplifier will be used for this probe, designed to minimize input voltage noise. This can be achieved by increasing the gate area of the input transistors and increasing the ratio of the gate lengths of the load and input transistors. This probe will be designed in both acute and 3D chronic versions.

There will also be some test structures of fold-down probes on this run. The layout is expected be finished in August. By that time, the MOSIS chip will come back and testing will begin.

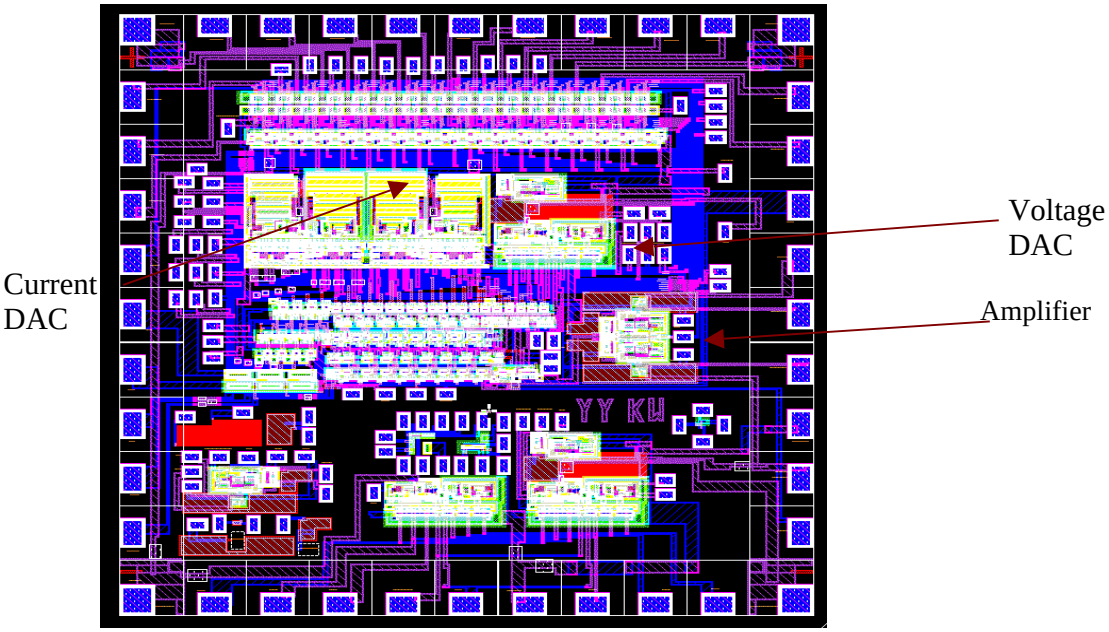


Fig. 6: Layout of the MOSIS chip

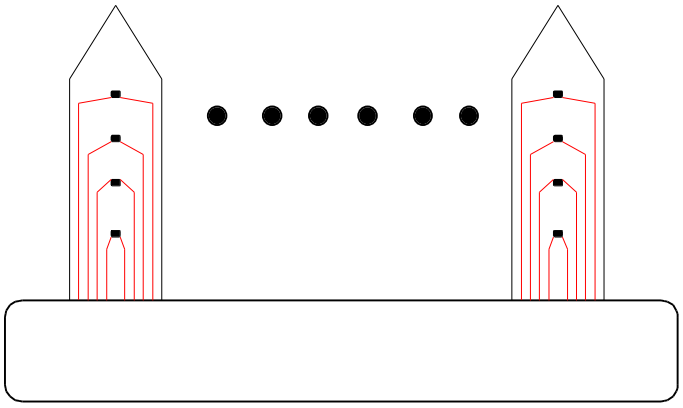


Fig. 7: Schematic showing the site routing on the 32-site active probe.

3. A Wireless CNS Stimulating System

The testing of the latest wireless system designed for stimulating probes, which started following the end of the University of Michigan's BiCMOS process run in December 2001, continued during this quarter. The previous quarter focused on testing and characterizing the power receiving and conditioning blocks such as the rectifier, regulator, and unity gain buffer, while during this quarter we mostly dealt with the data receiving and demodulating circuitry, trying to achieve the highest possible data transfer rates without sacrificing data integrity and system reliability. We are going to use functional chips in a larger system by assembling the different components of a wireless stimulating microsystem such as the transmitter circuitry, receiver/transmitter coils, and a PC-based command generation station. This report gives the results of this testing and characterization.

Clock Recovery Circuit

To minimize the rate of data loss over the telemetry link, the on-chip circuitry should be synchronized with the data transmitter block. Therefore, the internal clock was directly regenerated from the 4MHz carrier signal. The clock recovery block, which is shown in Fig. 8, is a ring oscillator whose self-oscillation frequency is altered by the carrier. Two small rectifier diodes provide an 8MHz unfiltered full–wave rectified version of the carrier. Usually, one of the diodes can be cut out to set the output clock at 4MHz. C1 and C2 form a capacitive voltage divider to protect the MOS gate oxides from the high voltage breakdown. The DC baseline across C2 is set around the inverter switching-threshold by the resistive feedback, and the AC component is adjusted by the high-pass filter combination of C1, C2, and M1 in the triode region. The transistor Q1 is added to bias M1 in the triode region and protect it against high input voltage. The self-oscillation frequency of the ring oscillator, which is dominated by the RC_3 time constant,

is tuned very close to the 4MHz carrier frequency after fabrication by cutting the links provided in the circuit layout, shown in Fig. 9. C_3 has two compartments that allow a choice between 2.3, 2.9, and 5.2pF and R has four 9.2kΩ compartments, one of which is initially in the circuit and the other three are shorted but allow us to increase it up to 36.8kΩ.

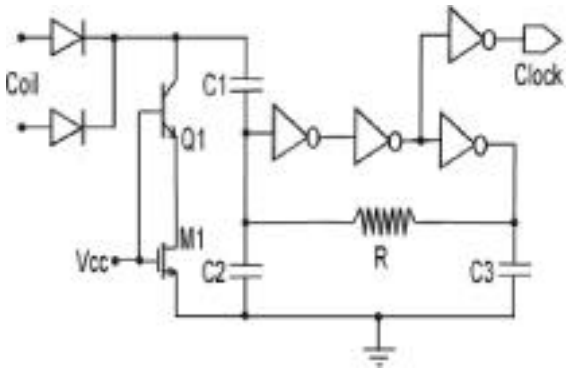


Fig. 8: Clock recovery schematic diagram

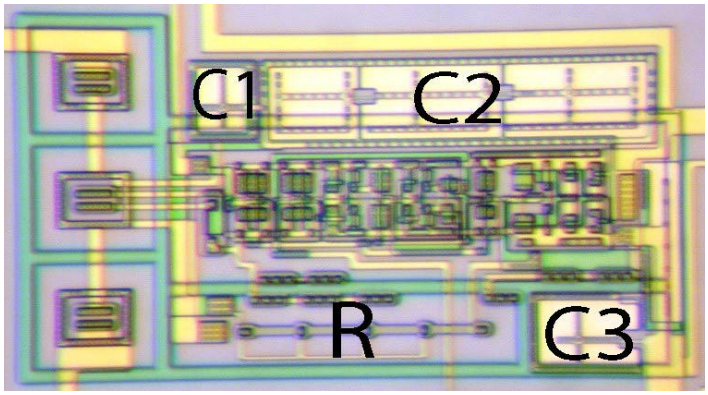


Fig. 9: The clock recovery block in Interestim-1 chip.

Fig. 10 shows variations of the self-oscillation frequency of the oscillator with the supply voltage. Increasing the supply voltage increases MOS transconductance and reduces inverter delays. Therefore, the oscillation frequency increases. When initially no links has been cut, we have C_3=5.2 pF and the oscillator frequency is 3MHz at Vcc=5V. In order to tune up the self-oscillation frequency at 4MHz, which is the desired carrier frequency, one capacitor compartment has been omitted to reduce C_3 to 2.9pF and the result is the upper curve in Fig. 10. In this situation, the ring oscillator is able to resume the internal clock generation even in case of losing the input 4MHz carrier baseline in case of a high amplitude modulation index, a problem that was seen in older clock regenerator designs and eliminated in this one. Fig. 11 shows the input and output waveforms of the clock recovery block. According to our measurements, when the self-oscillation frequency of the ring oscillator is set around 4MHz, it can follow the carrier

frequency from 2MHz up to 6MHz. The power consumption of this block could not be precisely isolated from other blocks but it is expected to be on the order of 0.5mW at 4MHz when Vcc=5V.

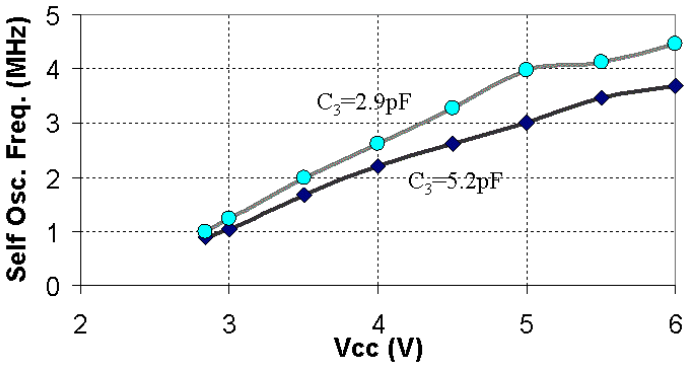


Fig. 10: Self-oscillation frequency of the clock generator ring oscillator vs. power supply voltage.

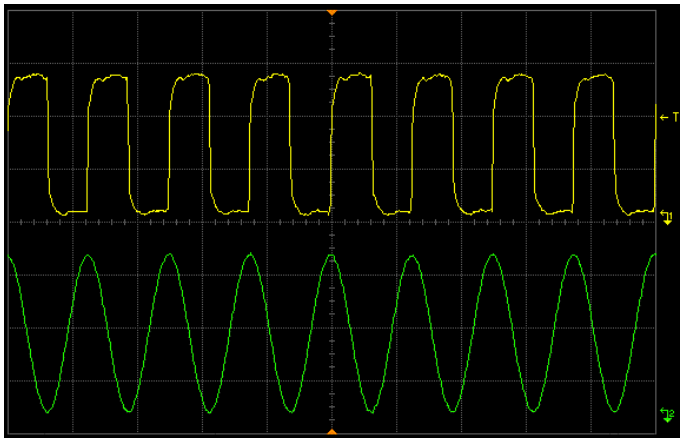
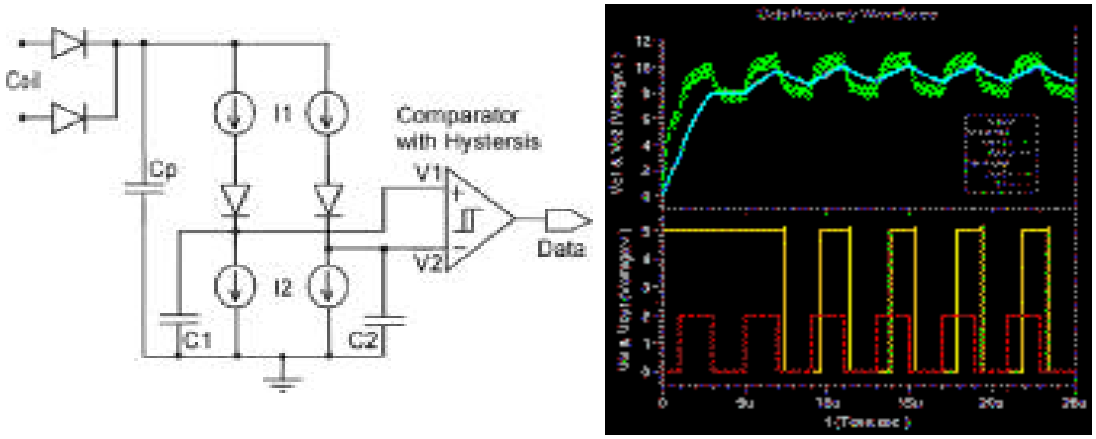


Fig. 11: The synchronous clock recovered from the received RF carrier signal at 4MHz

Data Recovery:

The Amplitude Shift Keying (ASK) technique has been used to transfer data along with the power transfer carrier to Interestim-1. The data recovery circuit employs a differential input current-mode circuit for reliable demodulation, which has been described in previous reports. Fig. 12 shows a simplified schematic diagram of the data recovery block as well as a simulated waveform sample. A full–wave rectified version of the carrier is low-pass filtered by Cp, whose cutoff frequency is set between the highest expected data rate (250Kbit/sec) and the 4MHz carrier frequency to obtain the baseband amplitude modulated carrier envelope. The I1 current source pair charge C_1=2pF and C_2=20pF, which have quite different values, with different time constants when the input envelope is high, and the I2 current sink pair discharge them with different time constants when the envelope is low. The upper traces in Fig. 12b show C_1 and C_2 voltages. V_{C1} has

a higher bandwidth with more ripple and sharper edges than V_{C2} with smoother variations. The capacitor voltages are fed into a hysteresis comparator circuit, and it gives the demodulated digital data signal at the output as shown on the lower traces of Fig. 12b. C_1 and C_2 time constants play an important role in the functionality of this circuit such as the maximum data rate that can be demodulated and the minimum modulation index that is required at each data rate for reliable data demodulation. Therefore, C_1 and C_2 are laid out with several compartments, as can be seen in Fig. 13, to be fine tuned for the carrier and data transfer frequency of choice after fabrication. C_1 and C_2 can be changed between 0.67 and 4.0pF and 5.0 to 40.8pF, respectively, covering a wide range of data transfer rates. Other important parameters in this circuit, which affect the time constant as well, are the I_1 and I_2 values. A single V_{Bias} DC voltage that initially was connected to VCC controls all of these current sources. Experiments showed that with a higher modulation index, the FSK demodulator circuit works with a wider range of V_{Bias} voltages as can be seen in Fig. 14. However, V_{CC} is usually out of the acceptable range except for V_{CC}=3V. Therefore, we had to apply an external V_{Bias} in the shown range to operate the circuit at V_{CC}=5V. This problem can be solved in later designs by adding a specific biasing chain to the data demodulator block with cutting links to adjust V_{Bias} in the desired range.



(a) (b)

Fig. 12: The data recovery block (a) schematic diagram and (b) sample simulation waveforms with the upper traces showing V_{C1} and V_{C2} and the lower traces showing the serial digital input (dashed lines) and demodulated digital output.

Fig. 15 shows the measured waveforms while demodulating a 4MHz carrier modulated with 100 kbit/sec data rate. The two upper traces are capacitor voltages, V_{C1} and V_{C2}, which are subtracted in a hysteresis comparator and generate the demodulated output waveform of the third trace. The lowest trace shows the ASK carrier input.

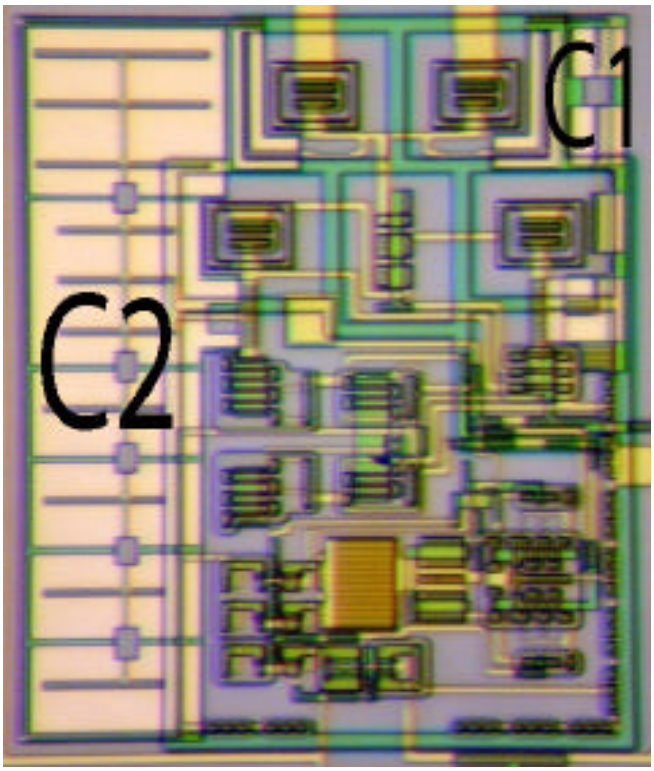


Fig. 13: The ASK data recovery block in Interestim-1.

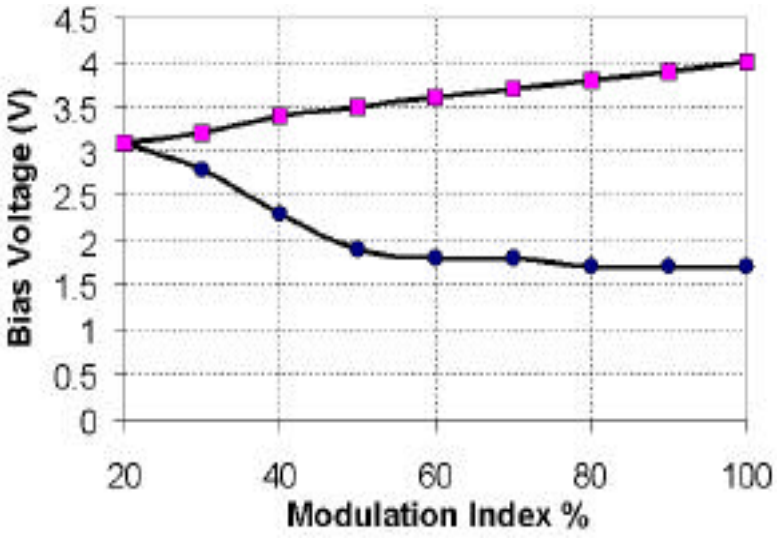


Fig. 14: Lower and higher limits of V_{Bias} for various modulation index values.

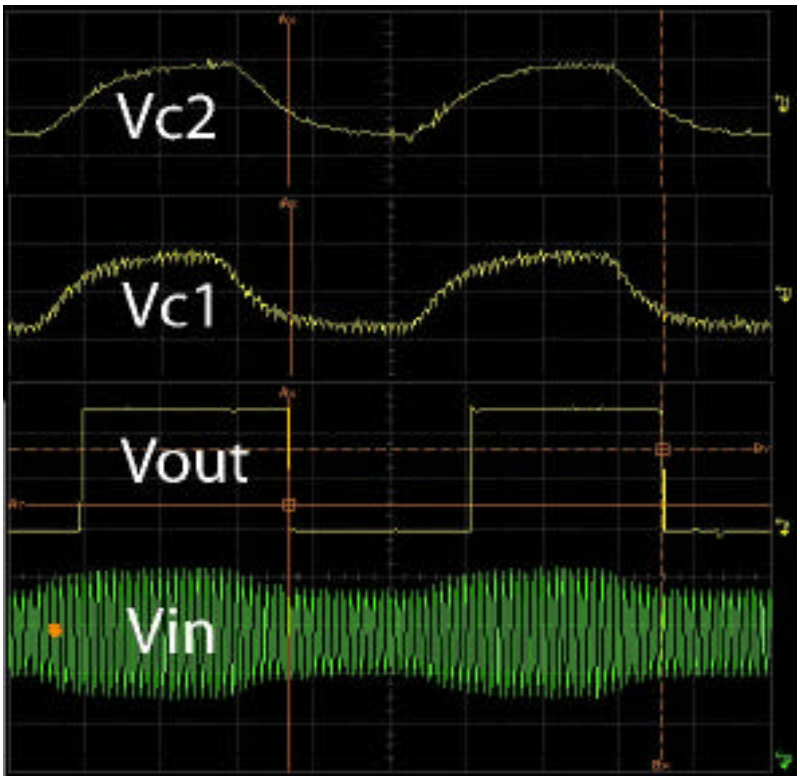


Fig. 15: Measured waveforms of 100kbit/sec demodulated data by FSK demodulator circuit.

DC-Level Shifter and Output Buffer:

The Interestim-1 output signals are DC-level shifted from 0-5V to 5V-10V to comply with the wireless stimulating microsystem power distribution approach shown in earlier reports. Fig. 16a shows the DC-level shifting circuit schematic, which performs this task in two steps. First, a cross-coupled differential pair shifts the logic levels from 0-5V to 0-10V and second, the 0-10V pulses are clamped at 5V. The DC-level shifter block gives three outputs; buffered 0-5V logic, 0-10V logic, and buffered 5V-10V logic. These waveforms are shown in Fig. 16b from the top to the bottom. This circuit utilizes positive feedback and does not have static power dissipation. Table 2 shows the delay values measured from input to the DC-level shifted output signal, which limit the maximum operating frequency of this circuit to 5.3MHz.

Power-on Reset:

The power-on reset is a safety feature in Interestim-1 design, which guarantees the whole circuitry to start from a known and stable initial state by activating the reset line for about 15μs right after the system power up to pass all of the supply rail and data line transitions before accepting any stimulation commands from the external transmitter. Fig. 17a shows a simplified schematic diagram of the Power-on Reset block. A reference

current source is mirrored to charge a capacitor. When V_C passes below a certain level, it sets the POR_ flag. Fig. 17b shows a photomicrogragh of this block on the interestim-1 chip. Fig. 17c shows sample measured POR waveforms when V_{CC} is connected to a square wave and Fig. 17d shows the measured start-up delay time variations versus the supply voltage.

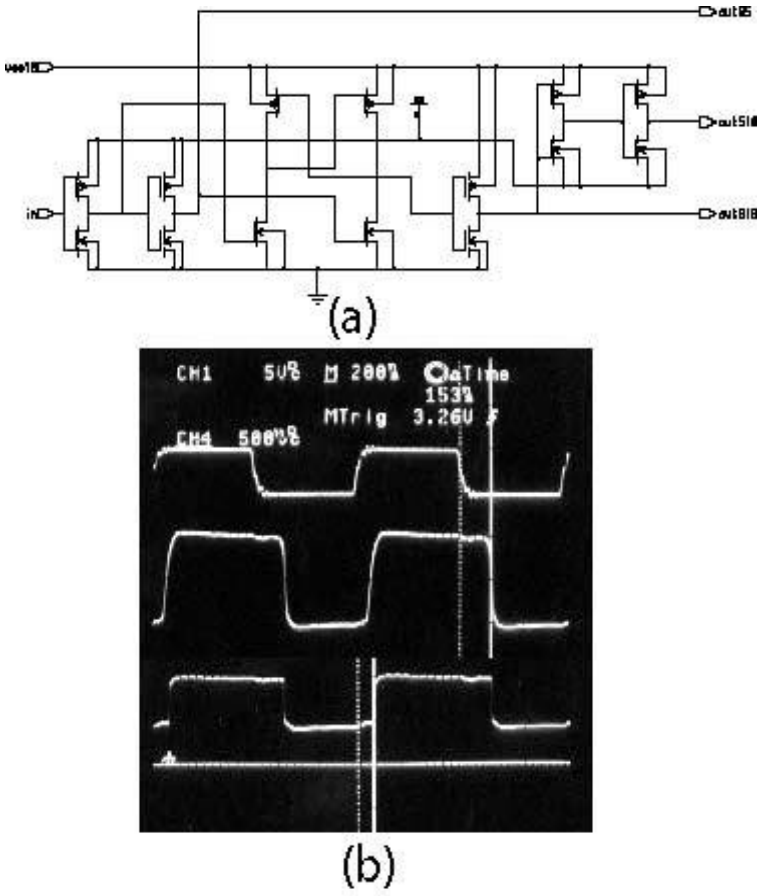
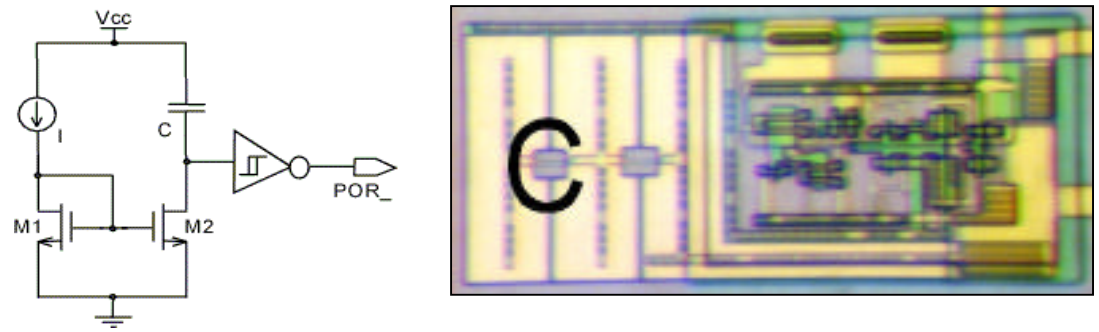


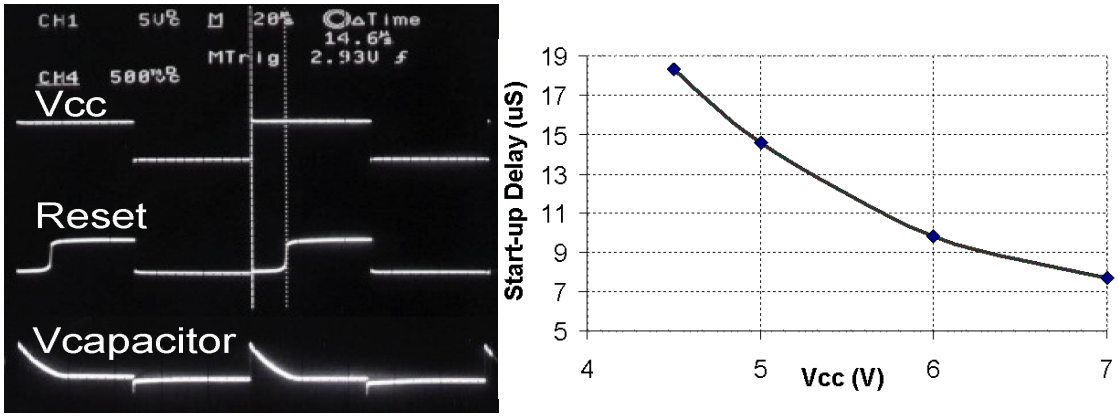
Fig. 16: (a) Two-step DC level-shifter schematic diagram and (b) measured 0-5V, 0-10V, and 5V-10V output waveforms.

TABLE 2
DC-LEVEL SHIFTER DELAYS

Output	**t_{LH} (ns)**	**t_{HL} (ns)**
OUT 0-10	66.4	151
OUT 5-10	75	182



(a) (b)



(c) (d)

Fig. 17: (a) The Power-on Reset simplified schematic (b) POR block on the Interestim-1 chip, (c) POR sample waveforms, and (d) Measured POR start-up delay with supply voltage variation.

Digital Control Block:

In processes with a large feature size, the digital circuitry rapidly grows and consumes a lot of chip area. Therefore, this block was designed very simple and efficient to save area and minimize dynamic power consumption. The digital control block diagram of Interestim-1 consists of several smaller blocks and is shown in Fig. 18. Some of the functions of the digital control block are as follows:

a) *Stepping-down the 4MHz clock extracted from the carrier, with a user selectable ratio to be synchronized with the data rate:* This function is performed with two

cascade counters and two comparators as can be seen in Fig. 19 in a block called digital2. The first 5-bit counter divides the 4MHz carrier-extracted clock down to 125kHz by a constant ratio equal to 32. The second 4-bit counter together with a 4-bit constant generator and comparator can divide the 125kHz clock by a variable ratio from 1 to 15 in order to generate an internal clock (ck50) from 8.3kHz to 125kHz. The internal clock frequency, which is the source of the Clock_out signal, should be at the same frequency as the transmitter data rate. The frequency selection is done by cutting links from the 4-bit constant generator block, which is shown in Fig. 19. Initially when all of the links are in place all of the outputs are high and the constant value N=15, which corresponds to 8.3kHz internal clock and data rate. When N1, N2, and N3 links are cut, N=1 and the internal clock will be 125kHz. The role of the second comparator in this block, which is designated by (≥) is to provide a 50% duty cycle square waveform for ck50 internal clock.

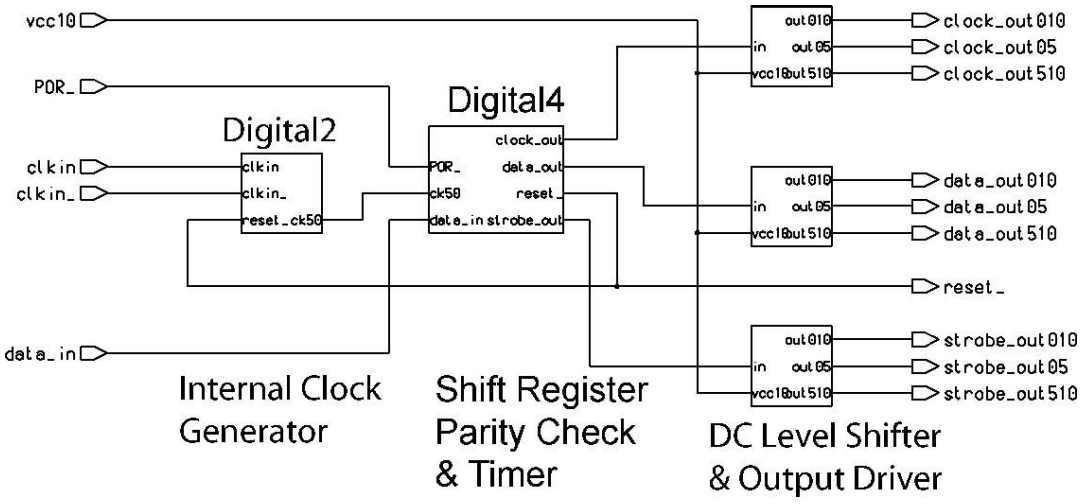


Fig. 18. Digital control block diagram in Interestim-1.

b) *Receiving the serial data bit stream from the data recovery block and temporarily storing it for parity checking:* The serial data bit-stream from the data recovery block enters a 9-bit serial shift register, which is part of the digital4 block and is shown in Fig. 21. This shift register is connected to a 9-bit parity-checker circuit, which can be seen in Fig. 22. Parity checking, a typical wireless systems safety feature, is included in this chip to verify data integrity. It activates at the 9th bit of each frame, which is the parity bit. A wrong parity bit generates a reset pulse and returns the Interestim-1 circuitry to its initial state without transferring any wrong stimulation command to the STIM microprobe. Therefore, it can also be used as a mean of resynchronization with the external transmitter system by sending an intentional wrong-parity command. This will be described in further detail below.

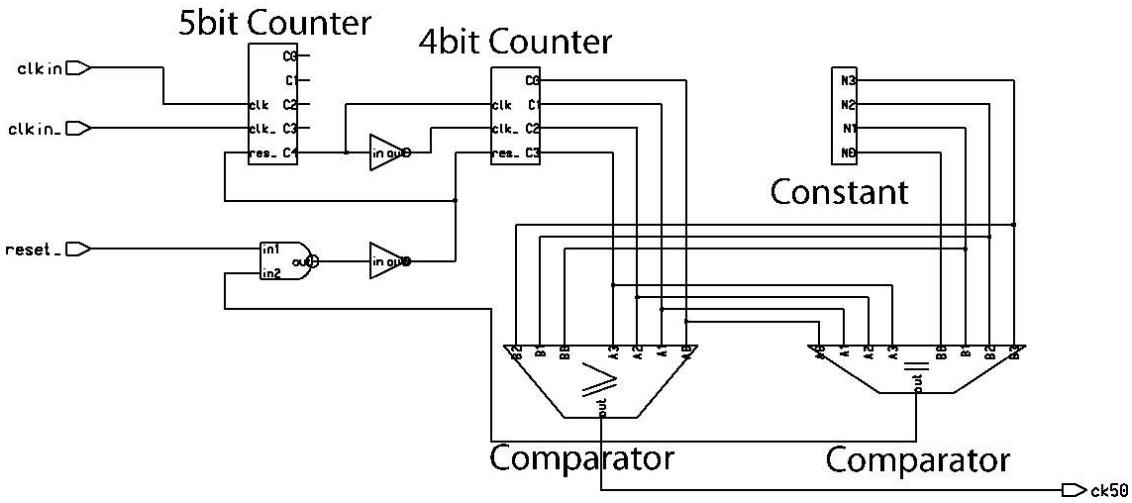


Fig. 19: The 4MHz clock extracted from the carrier by the clock recovery circuit is divided down to 8.3kHz ~ 125kHz by two cascade counters to generate the internal clock, which will be synchronized with the recovered data to generate the Clock_out signal.

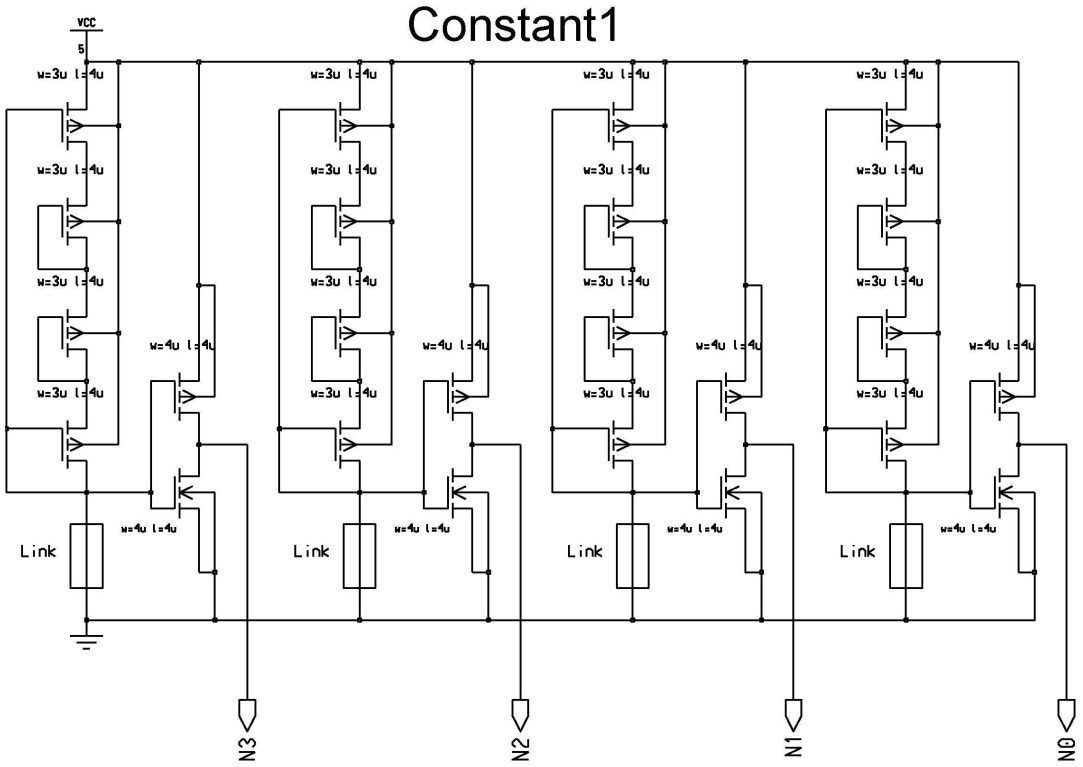


Fig. 20: 4-bit constant generator circuit with very small static power consumption.

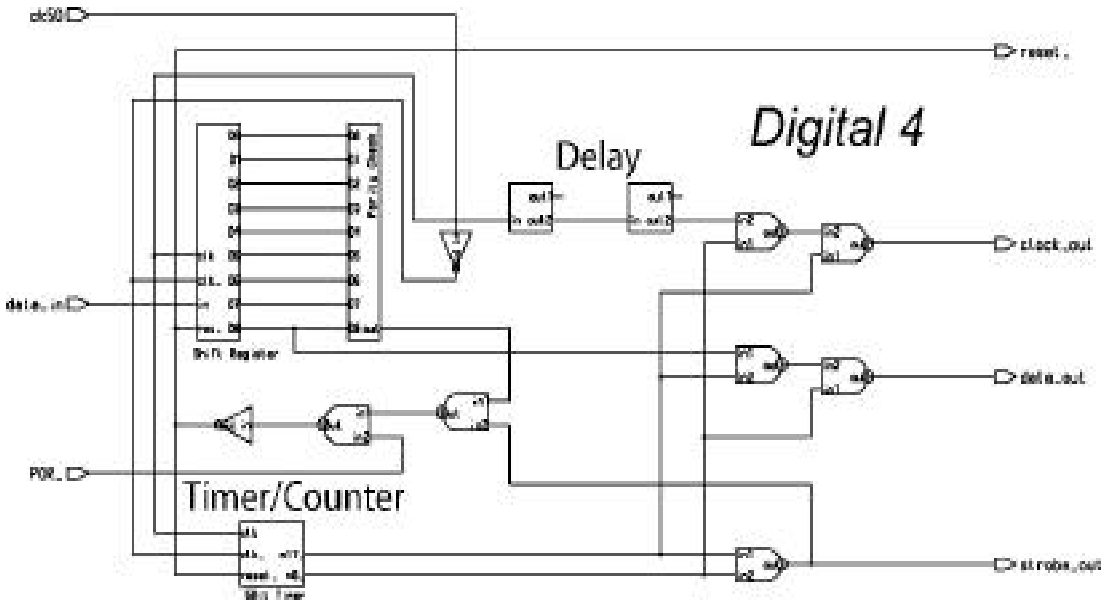


Fig. 21: Digital4 block diagram containing parity checking and timer/counter blocks, which provide output signals according to the STIM-2D data transfer protocol.

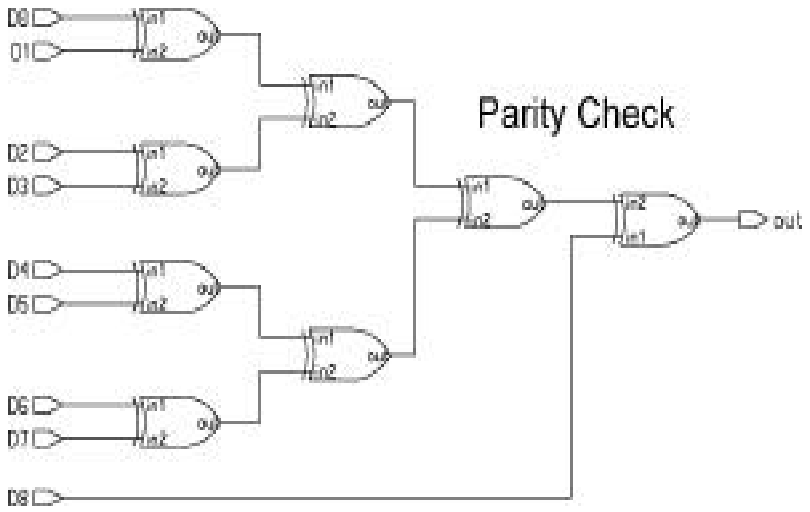


Fig. 22: 9-bit parity checker circuit.

c) *Generating a clock pulse for every single data-bit and a synchronizing strobe pulse for every single data-frame of 9 bits, and finally sending all three of these signals to the DC-level shifter blocks according to the STIM-2D data transfer protocol shown in Fig. 23:*

A timer/counter circuit counts ck50 pulses and sets n8_ and n17_ flags at the 9th and 18th bits of each command respectively. The n8_ flag forces Clock_out output signal to go

low and Data_out output signal to go high at the 9th bit of each command corresponding to the STIM-2D protocol of Fig. 23. Similarly, n17_ forces Clock_out to go high and Data_out to go low at the 18th bit of each command and finally both of these flags generate strobe timing pulses on the Strobe_out output signal. In order to test the entire digital control block apart from the rest of circuits we included a prototype test chip, shown in Fig. 24, on our wafer. Besides, we needed a serial digital pattern ganerator, which is described in the next section.

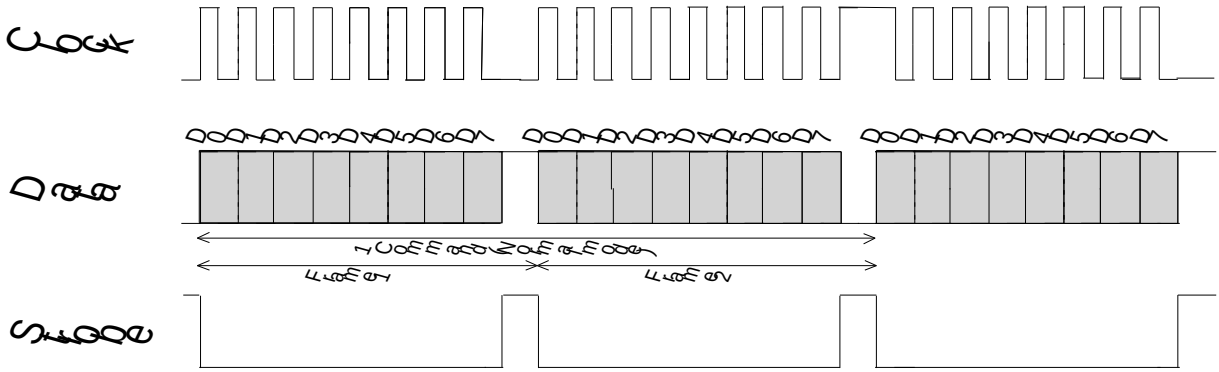


Fig. 23. The STIM-2D data transfer protocol.

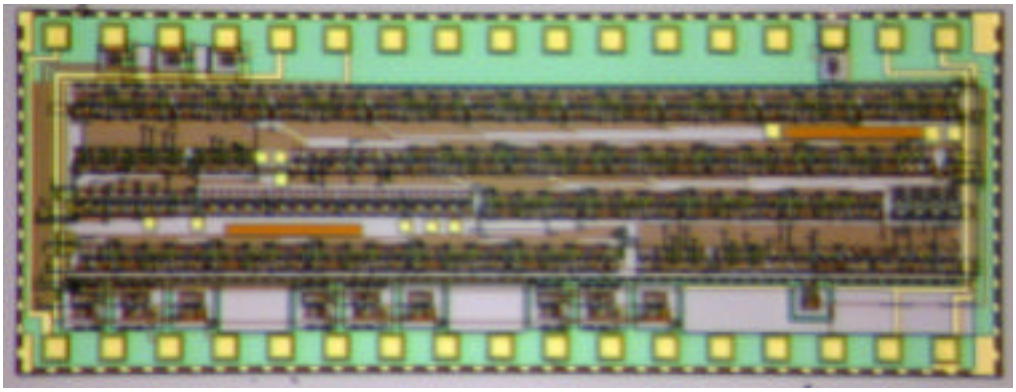


Fig. 24. Interestim-1 digital control prototype chip.

PC-Based Serial Command Generator:

In the experimental wireless stimulation setup, stimulation, addressing, and control commands are being generated by a PC-Station running a graphical user interface (GUI) software. The GUI was developed in the LabView-6 environment and to generate the serial command bit-stream, the PC-Station was equipped with NI PXI-6070E general-purpose data acquisition card from National Instruments Corporation, which is shown in Fig. 25. This card has 16 analog-inputs, 2 analog-outputs, and 8 digital I/O lines. Analog

input and output channels each have 12-bit amplitude resolution and up to 1Mega-sample/sec timing resolution. To generate the serial command bit-stream either digital or analog outputs could be used since we needed only two channels, one for serial data and the other for synchronous clock. However, using the analog output was advantageous due to controlling the serial bit-stream output amplitude through the GUI software. By using both analog output channels simultaneously, the output samples were divided between these two channels and each channel could reach a maximum rate of 500 k-sample/sec. Therefore, the maximum clock frequency was limited to 250kHz while the digital block had been designed based on a 4 MHz input clock from the clock recovery circuit. Therefore, the next version of the PC-Station and its GUI will be based on NI PXI-6533 high-speed digital I/O card, which has a timing resolution of 20MHz and is capable of providing 4MHz synchronous clock and data patterns simultaneously for testing the Interestim-1 and 2 digital circuitry.

Fig. 25: NI PXI-6070E from National Instruments was used to generate serial command bit-stream.

Figure 26 shows the front panel of the first GUI called analog pattern generator-1 (APG1), which is capable of generating two individual analog or digital output patterns based on the values entered in channel 0 and channel 1 matrixes. The user also specifies the number of words in each frame, number of iterations, output signal amplitude, polarity of channels, and sample generation rate. The input matrixes are dimensioned N×9 with the first bit assigned to parity in order to comply with the Interestim-1 data structure. In order to provide the user with a feedback of what is being generated at the output channels, both serial bit-streams are shown on the lower part of the panel under the Output Array label. Fig. 27 shows the APG1 visual block diagram. Two N×9 input

matrixes are multiplied by the selected amplitude, combined, and re-dimensioned as a 2×9N matrix, which is loaded into the analog output data-buffer.

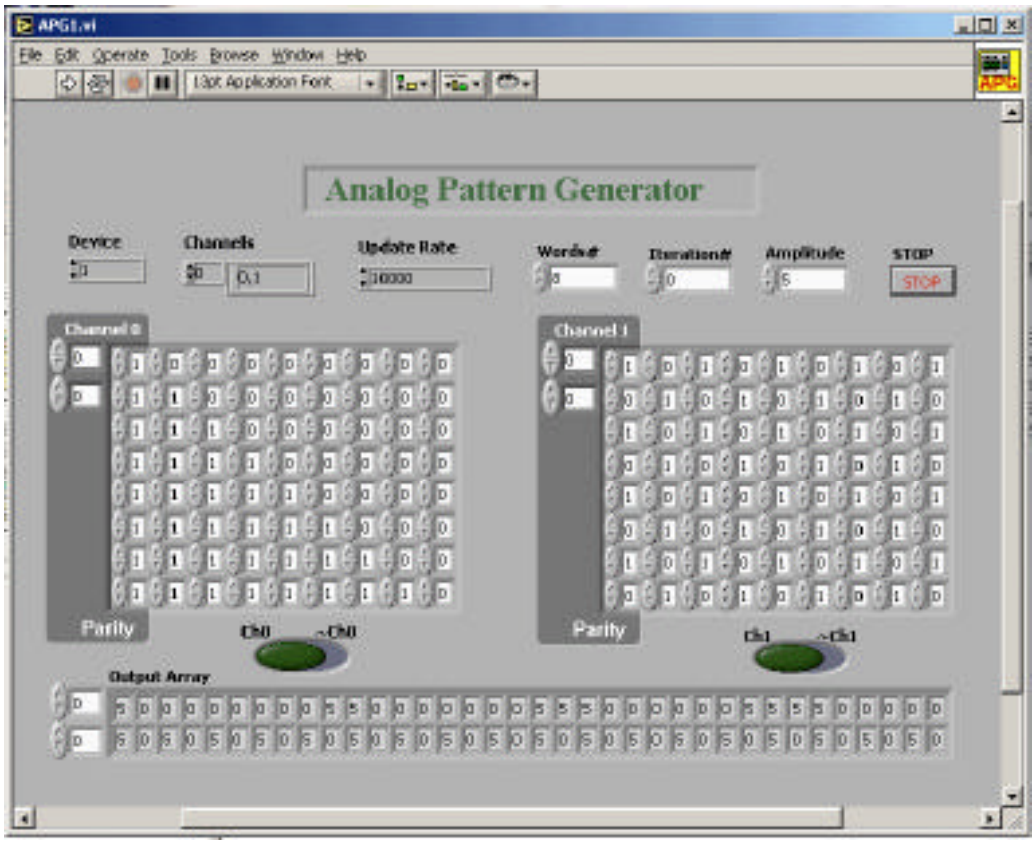


Fig. 26: The graphical user interface (GUI) software called analog pattern generator-1 (APG1), which was developed in LabView-6 environment and used in the stimulator experimental setup to generate a serial command bit-stream.

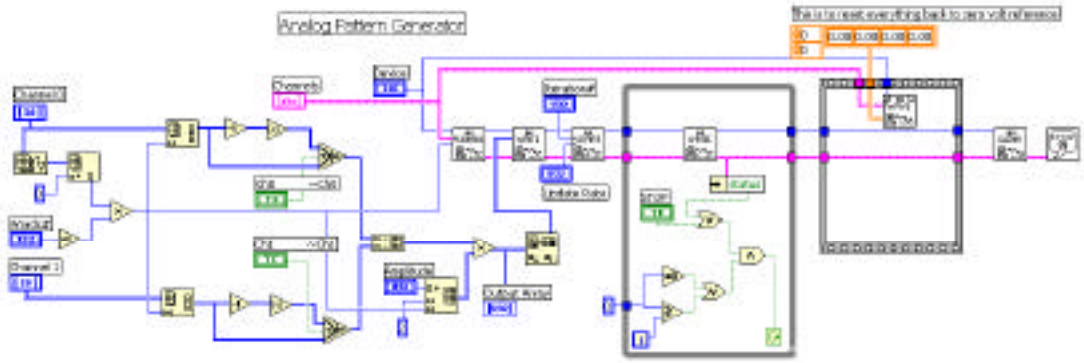


Fig. 27. The analog pattern generator-1 (APG1) visual block diagram.

A newer version of the APG software was also developed which is capable of generating the synchronous clock signal automatically based on the user-defined specifications of the serial data pattern. Two new features were added to this version to facilitate testing. First, a certain number of clock cycles (Clock#) could be generated for every single bit of data to consider the effect of frequency dividers in the digital control block shown in Fig. 19. Second, a certain number of preamble frames could be generated before entering the main loop of iterative command generation. As mentioned in section 6b, these preamble frames, which are simply data bytes with intentionally wrong parity bits, can be used to reset the entire Interestim-1 chip whenever the external transmitter system wants to resynchronize with the implanted stimulator chip. Fig. 28 shows the APG3 graphical user interface panel, and Fig. 29 shows its visual block diagram in LabView-6.

The Interestim-1 digital control block, discussed above, was tested by supplying clock and serial data bit-stream from the PC-Station running APG3. Fig. 30 shows sample measured waveforms at low frequency (only for testing) with Clock_in, Data_in, Clock_out, and Data_out signals from the top to the bottom traces. The input data has been pulse width modulated with the ASK carrier having high amplitude in 25% and 75% of a bit-period when zeros and ones are being sent respectively. The data bit value is red at the rising internal clock edge, which comes right at the middle of a bit period. This extra modulation scheme is not necessary for this design but it can be employed as a synchronization feature to improve system reliability in later designs.

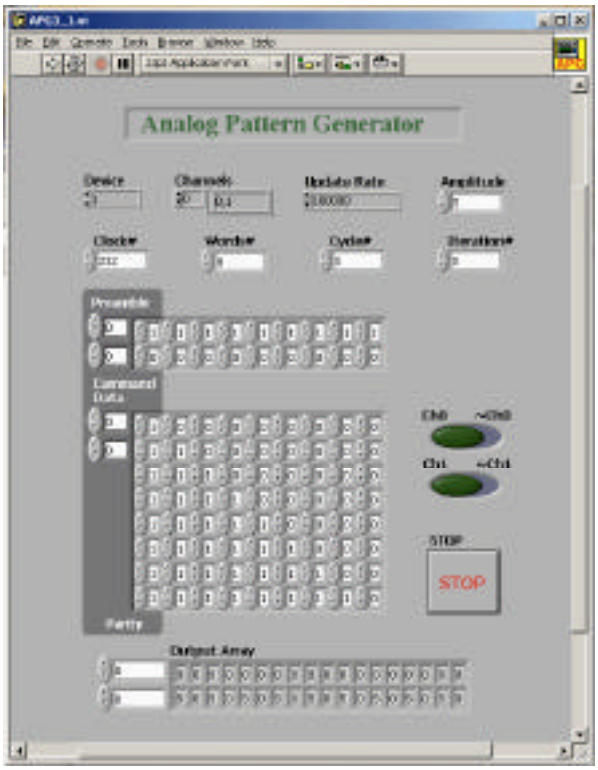


Fig. 28: The APG3 graphical user interface panel.

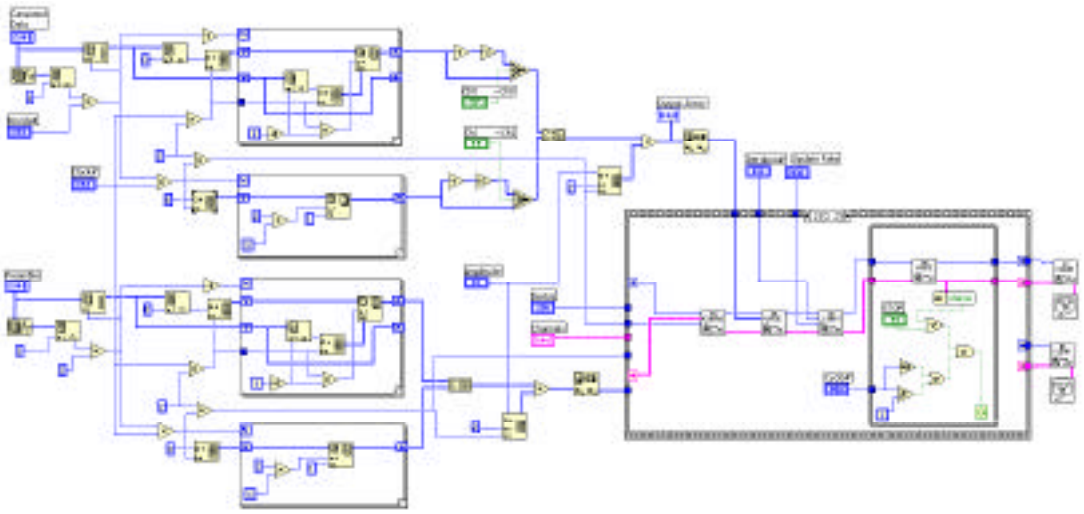


Fig. 29. The analog pattern generator-3 (APG3), visual block diagram.

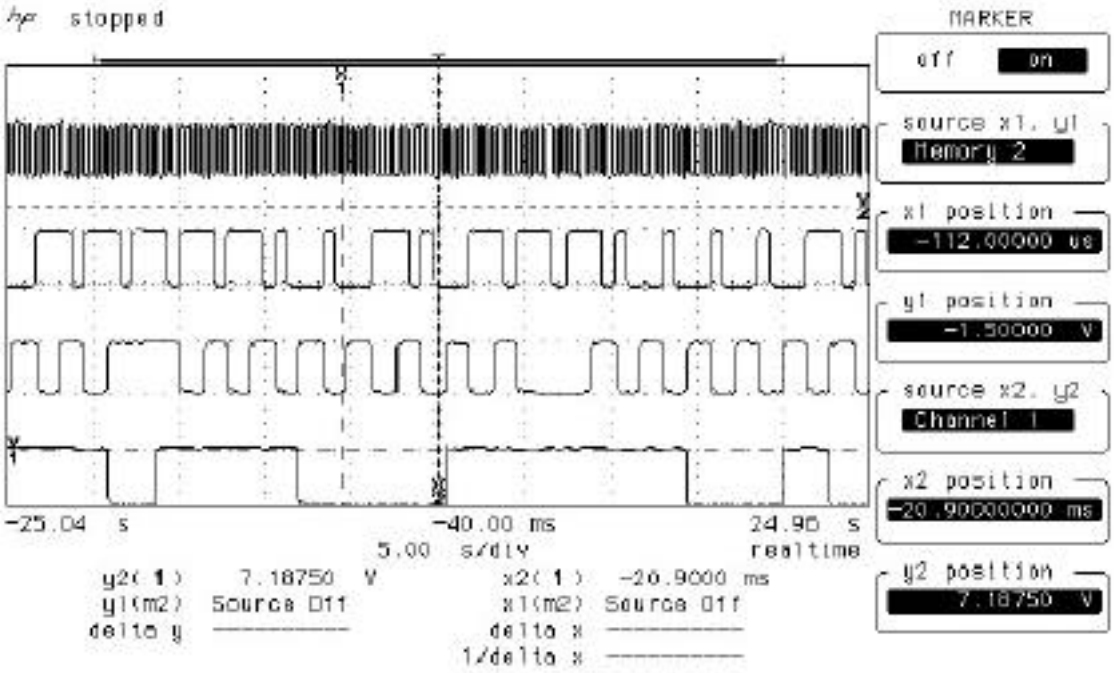


Fig. 30: Sample measured waveforms into and out of Interestim-1 digital block showing Clock_in, Data_in, Clock_out, and Data_out from top to bottom.

Fig. 31 is another measured example showing the input bit-stream on the lowest trace in green and the resulting output signals: Clock _out, Data_out, and Strobe_out from top in yellow traces. Comparing Fig. 31 measured waveforms with the STIM-2D data transfer protocol shown in Fig. 23 indicates the correct functionality of digital

control block. It can be seen in Fig. 31 that every input byte of Data_in shows up on Data_out output line with 9 clock cycles delay, which is because of the 9-bit shift register of digital4 block shown in Fig. 21.

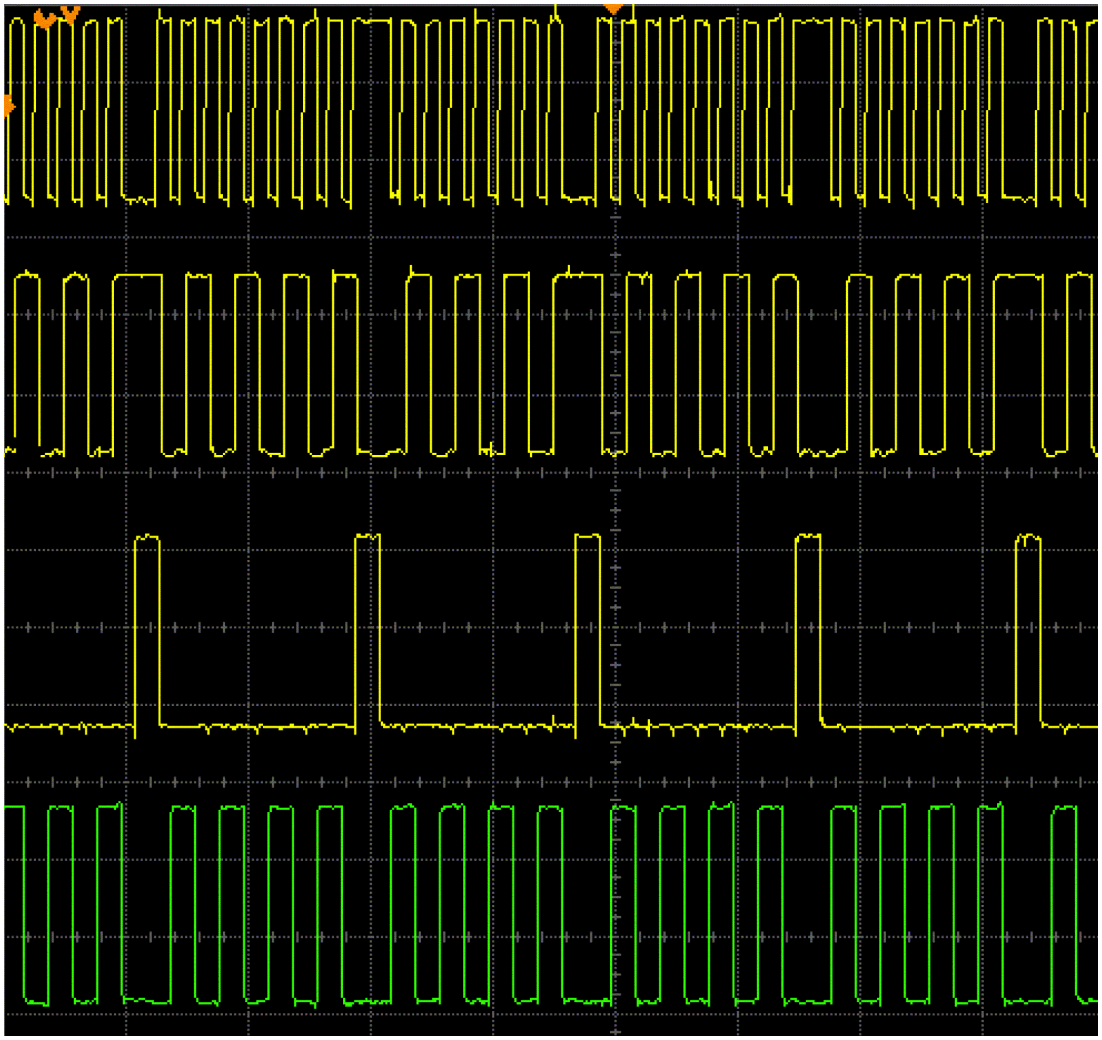


Fig. 31: The Interestim-1 measured output signals (5V-10V logic level) at 100 kBit/sec. Every input byte shows up at the output with one frame delay because of the 9-bit shift register in digital4.

During the next quarter we will try to operate the entire Interestim-1 and Interestim-2 systems self sufficiently with the two receiver-coil nodes as the only inputs. We are going to work on the transmitter circuits and improve the PC-based command generator station to achieve higher data rates in order to implement a true wireless stimulating setup for testing the functionality of our chips in vitro.

4. Conclusions

During the past quarter, work has gone forward in two principal areas. We have explored approaches to reducing the circuit on our high-end stimulating probes, and we have continued in our efforts to develop a wireless interface to these probes. There has been substantial progress in both areas. A chip containing the circuitry for a two-channel 16-site active probe has been designed in a 1.5µm n-well 2M/2P CMOS process and submitted to MOSIS for fabrication. This chip will be useful with passive stimulating probes, both in acute implementations (mounted on the supporting stalk) and in chronic use (on the platform). It will also serve to confirm the operation of several important circuit blocks. The chip contains five operating modes: site activation, impedance tests, normal stimulation, recording, or anodic bias set. Each command consists of 16 serial bits. We have also designed a four-channel 32-site active probe for fabrication this fall. It incorporates extensive self-test capability, current-output digital-to-analog converters that are much smaller in layout area and that incorporate a shared bias string whose current levels are independent of bias.

In the wireless area, we have continued to test the most recent circuit chips at high data rates. The circuitry can generate an on-chip clock at 4MHz with power dissipation of about 0.5mW, following the carrier from 2MHz to 6MHz. The data recovery circuit performs well at 100kbit/sec data rates, and likely much higher. The dc-level shifter circuitry correctly produces voltages at 5V and 10V, consistent with using a 10V power supply swing to produce ±5V biphasic stimulus signals. The power-on-reset function is likewise fully functional. The digital control block permits internal clocks from 8.3kHz to 125kHz to be derived from the 4MHz input carrier. It also performs parity checking on the serial data bit stream from the data recovery block and formats the data together with a strobe for use by the probe circuitry. In order to test this circuitry, a PC-based command generator has been implemented. This system will also be important in testing the full wireless probe system, which we hope to do during the fall quarter.